Digging into SiC etch

Silicon carbide is an extremely challenging material to etch, with dry processes apparently limited to etch rates of about a couple of microns per minute. While laser drilling is an option, production rates are slow, given the small numbers of features that can be formed at a time (one or at most a few per cycle). Two groups of researchers, at Fujitsu and TriQuint, have been looking at some problems of etching back-side via holes in SiC substrates. Mike Cooke reports.

High-thermal-conductivity silicon carbide is an attractive substrate material for power applications such as lasers and power amplification of high-frequency radio/microwave signals. High thermal conductivity allows better dissipation of the heat created in power devices. However, not only is the material difficult to grow (and hence expensive), it is also difficult to work, since the material has hardness properties close to that of diamond.

For plasma etch, a nickel mask is often used. This can achieve selectivity rates for SiC etch of 45:1. Etch rates have been improved from initial attempts giving less than 0.6μm/min to the 2.7μm/min achieved more recently (2005) by Surface Technology Systems (STS, now SPP Process Technology Systems, or SPTS).

For power transistors, improved electrical performance can result from creating back-side through-substrate via connections to transistors produced using the wide-bandgap properties of SiC itself, or by adding III-nitride layers. To produce such via holes, the wafer is generally ground down mechanically and then polished. This reduces the distance needed to etch the hole and also makes the substrate more thermally conductive between the device layer and heat sink arrangements.

Fujitsu researchers have reported on their work to overcome some of the problems of reactive ion etching (RIE) of SiC material with a view to creating back-side via holes for gallium nitride (GaN) high-electron-mobility transistors (HEMTs) [1].

One strange effect the Fujitsu team dealt with was the formation of pillars in the via hole (Figure 1). The researchers believe that these structures form on the end of micro-pipes that are created in the original growth of the SiC material (Figure 2). Micro-pipes are empty tubes in the SiC material. Their ends have a slower etch rate than the surrounding SiC material, and further problems for etching arise from byproducts of the etch being deposited on the micro-pipe cap. These byproducts create the pillars that consist of a chemical combination of nickel from the mask and SiF_x from the etch process.

Some firms (e.g. Cree) supply 'micro-pipe-free' material, at a price, where this effect should not be a problem. However, for those not using such material, these pillars form a barrier to proper metallization of the via-holes and should be eliminated. The researchers found that reducing the pressure to about 5Pa eliminated the pillars by enhancing Ni desorption and an oxygen flow of 20sccm reduced micro-trenching effects that can occur at lower pressures.

The Fujitsu team also comment that it is best to keep the via holes uniform in size to avoid 'lag' effects where

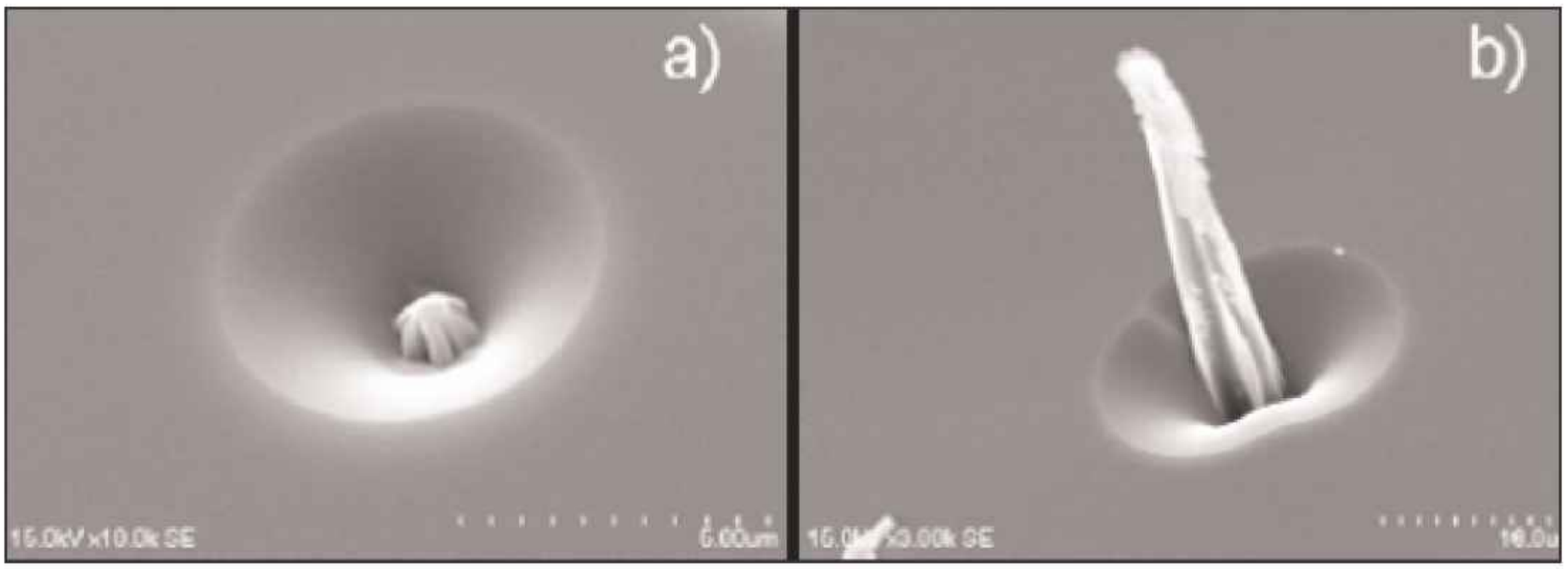

Figure 1. Example of pillar formation during etch of via hole in SiC.

small-diameter structures etch more slowly than large ones. It is also important to remember that doped and semi-insulating wafers etch at different rates. On the basis of their work, Fujitsu developed a process to etch SiC via holes at a rate of 2μm/min (Figure 3).

TriQuint has also been looking into SiC etch for via holes [2]. It is more interested in etch process sustainability, and so dialed the rate back to about 1μm/min. Opening up the etch chamber for wet cleaning with chemicals such as chlorine (Cl_2) and boron trichloride (BCl_3) can substantially deteriorate subsequent etch performance.

Like Fujitsu, TriQuint has problems with pillar formation that it attributes to micro-masking inside the via being formed. Returning the etch chamber to its initial performance required replacement of some parts, costing time and money. These problems must be overcome for the etch process to become part of a mass production environment.

The researchers carried out a series of experiments on 1cm^2 pieces in an STS inductively couple plasma (ICP) etch system. The SiC was an n-type 6H polytype. There were further samples of GaN/SiC and Ni/Si used for selectivity and etch rate studies. Pillar formation was studied on SiC samples that had previously been ground down by 10μm and then polished a further 1μm.

The researchers found that SiC etch rates were relatively constant with respect to the RF coil power (1500–2500W), but that the rate increased with increased platen power (150–300W). However, low coil powers did result in severe pillar formation. But, even at high powers, pillars persisted in some isolated vias. Hence, pillar formation at low power is attributed to the process parameters, while at high power it is attributed to the surface condition of the particular sample.

In terms of SiC-to-GaN selectivity, the results were relatively insensitive to platen power, but improved with coil power. However, the TriQuint researchers point out that a modest selectivity of ~25 is sufficient to stop the etch when it reaches the GaN layers, and that there is not much benefit to increasing the RF coil power to achieve more than this. Further, high coil powers can lead to thermal and mechanical stress, causing failure of the ceramic parts used to isolate the coil from the rest of the chamber. The SiC-to-Ni selectivity was greater than 50 for the whole range of powers tested.

Another factor affecting pillar formation was the carrier. For example, gross pillar formation was not observed with a Ni-plate Si carrier. With a Ni/sapphire carrier, intermittent pillars were observed. A Ni/glass carrier had the worst performance after Cl_2/BCl_3 cleans, with repeated pillar formation. The sample temperature is believed to affect pillar formation, and it is to be noted that Si has the highest thermal conductivity and glass the lowest. Temperature measurements suggest the sample temperature was ~80°C for silicon and sapphire carriers, but increased to ~110°C for the glass carrier.

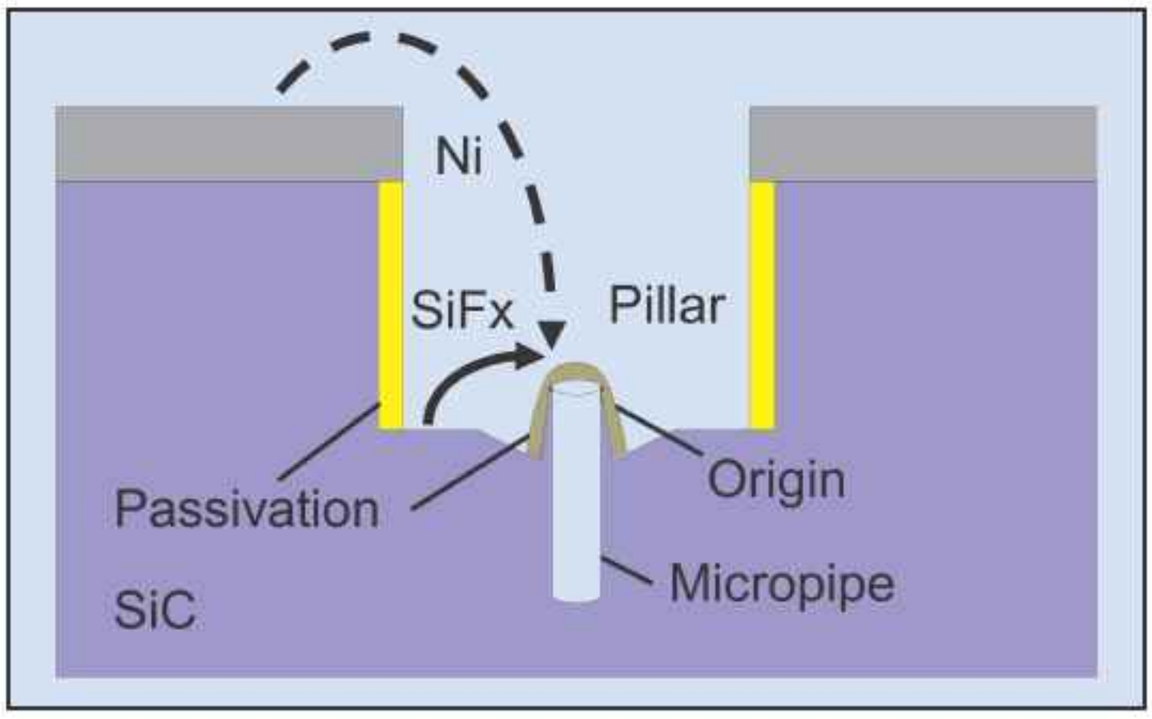

Figure 2. Fujitsu view of pillars forming on micro-pipes.

'Seasoning' a chamber before use with oxygen and sulfur hexafluoride (SF_6) can reduce gross pillar formation. The pre-etch sputter clean used to break through the surface and begin the etch is also important, since a significant amount of Ni can be generated that is then deposited on the chamber wall and back onto the sample surface, including in the via areas. This sputtering is increased at higher temperature, offering a partial explanation of why pillar formation is more severe on glass carriers. ■

References

1. Naoya Okamoto et al, CS Mantech 2009, 'SiC backside via-hole process for GaN HEMT MMICs using high etch rate ICP etching'
2. Ju-Ai Ruan et al, CS Mantech 2009, 'SiC substrate via etch process optimization'

Figure 3. Fujitsu process for SiC via-hole etch.